

**Amendments To The Specification**

Please replace the paragraph beginning on page 13, line 9 with the following amended paragraph:

Switch SW3 routes the output of RF to IF converter 1003 on either to AMPS SAW filter 1011 or to CDMA SAW filter 1012, which provides band limiting.

Please replace the paragraph beginning on page 13, line 9 with the following amended paragraph:

Level detector 102 can be any type of circuit that is able to detect changes, over an appropriate time frame, in the signal level with which the receiver is currently operating. For example, level detector 102 can be a rectifier, or a heat generator of some type coupled to a heat monitor such as a thermsistor thermistor.

Please replace the paragraph beginning on page 48, line 4 with the following amended paragraph:

[[An]] A second approach is to move the transmission rejection filter into the bypass path. Using this architecture, the point at which one of the amplifiers is switched in and out, i.e. the bypass point, can be lowered to the insertion loss of this filter, which can be about 2 dB, for example. This can allow the bypass point to be about -91 dBm. Such a bypass point can be less than the -90 dBm extended jamming signal test described above.

Please replace the paragraph beginning on page 15, line 13 with the following amended paragraph:

In embodiments of the invention that use bias adjustment circuit 105, it adjusts, filters, amplifies and/or conditions bias control signal 140 into adjusted bias control signal 141, which is then used by bias generator 103 to generate bias level 143. The adjustment or adjustments applied may include any transfer function, preferably but not necessarily monotonic,

including but not limited to conditioning, filtering, clipping, expanding, amplifying, dampening, scaling, offsetting, band limiting, sampling and holding and/or summing with [[an]] a DC offset.

Please replace the paragraph beginning on page 52, line 7 with the following amended paragraph:

The bias adjustment function is performed by bias level ~~comparitor~~ comparator 810, sample and hold circuit 811 and bias difference circuit 812.

Please replace the paragraph beginning on page 52, line 9 with the following amended paragraph:

Bias level ~~comparitor~~ comparator 810 can be any type of circuit that is able to generate regulating feedback signal 842. In particular, regulating feedback signal 842 can be generated by comparing a reference voltage against a signal internal to bias generator 803. In the embodiment shown, the reference voltage is formed by a two resistor voltage divider between Vcc and ground, which helps compensate for variations in Vcc.

Please replace the paragraph beginning on page 53, line 9 with the following amended paragraph:

FIG. 9 is a circuit diagram and [[an]] a pin out diagram of an application specific integrated circuit (ASIC) for bias control according to one embodiment of the invention. As shown, many of the electronic circuit components of FIG. 8 are formed within a single integrated circuit having 10 pins. Implementing these circuit components as an ASIC can reduce manufacturing costs and complexity of receivers that use reactively biased front end circuits.